JSATS Tag downsize project progress report No. 1

Report Date: February 28, 2011

Prepared for: US Army Corps of Engineers, Portland District

Prepared by: Pacific Northwest National Laboratory

Comment: This is the first of a series of monthly progress reports on the conduct of the JSATS Tag downsize project. The purpose is to provide the Portland District with a periodic summary of accomplishments, planned activities, and issues.

To date, we have been focusing preparing, reviewing and finalizing the application space of the downsize tag and determining the power requirements of the tag. The project team presented our overall goal and strategy and discussed various tasks for this project at 2/14 FFDRWG in Portland.

Summary:

Time period	**Accomplishments**	**Planned Activities**	**Issues**
	1/1/11 to 2/28/11	**3/1/11 to 3/31/11**	
Application space	Put together application space at FFDRWG meeting on 1/19. Reviewed the list and made recommendations about the functionality to include in the downsized transmitter on 2/14.		None
ASIC/ Circuitry	Developed an initial set of specifications based on the application space review. Some questions were deferred for further analysis: (i) whether to use acoustic or radio frequency signals to program the tag, and (ii) how best to incorporate the passive integrated transponder. Measurements are underway to resolve these questions. Measured the electrical response of the crystal, the driving voltage necessary to produce the required sound pressure level, and the overall power consumption. Developed a circuit model of the transmitter and used it to cross-check the power consumption numbers. This information is vital to select the appropriate ASIC fabrication technology and determine the voltage and current requirements. Started the design of a timer circuit that consumes minimal power, yet achieves the necessary accuracy.	We will take further measurements so we can make the final selection between the various options. We also plan to submit an initial test ASIC for fabrication in April. This ASIC will include components such as the PZT driver and timer circuits so we can better characterize their performance.	None

Time period	Accomplishments 1/1/11 to 2/28/11	Planned Activities 3/1/11 to 3/31/11	Issues
Batteries	Measured the working parameters of 337 battery installed in the present tag for working current and voltage as time changes to baseline the requirements for the new battery design. Investigated the feasibility of a lithium battery and possible designs for the JSATS as a smaller source with the required capacity. Investigated the merits and drawbacks of cathode material for the new battery under development to meet or exceed the 337 battery: CF_x, Silver vanadium oxide, Sulfides (MoS_2, FeS_2 etc.), Oxides (MnO_2 etc.)	The Swagelok battery test cell is near complete. The remaining parts required are cutters for the stainless steel spacer and the lithium anode. Once complete, cells designs with selected cathode material will begin.	None
Form/ packaging	Investigating a capsule type of packaging to simplify the process and reduce cost, as well as method to improve the current Parylene C potting process. Both methods will be investigated for fabrication, performance and manufacturability.	Locate and purchase capsules to begin performance testing. Investigate equipment at PNNL for vacuum deposition of Parylene C coatings.	None
Ceramics/ Transducer	Ordered various PZT materials from several vendors. Measured the voltage required to power up existing transducers.	Investigate the feasibility of the materials for JSATS tag frequency and source level	None

JSATS Tag downsize project progress report No. 2

Report Date: March 31, 2011

Prepared for: US Army Corps of Engineers, Portland District

Prepared by: Pacific Northwest National Laboratory

Comment: This is the second in a series of monthly progress reports on the conduct of the JSATS Tag downsize project. The purpose is to provide the Portland District with a periodic summary of accomplishments, planned activities, and issues.

Summary:

Time period	Accomplishments	Planned Activities	Issues
	3/1/11 to 3/31/11	**4/1/11 to 4/30/11**	
Code space	Due to limitation of JSATS transmitter codes, we are evaluating ways to control code space. Right now we have 65k codes available and we usually use half of them. This year USACE Portland district will use >25k codes. At the meeting on 3/22, we communicated the options identified for expanding the number of available codes. Discussion revolved around the feasibility of implementation in the downsized tag, in existing receivers, and in post processing. The primary options proposed are: 1) Different baker code or possibly longer one (11-bit). 2) Longer data bits. One 4-bit data digit increases the number of tag codes to 1M. We may also need to increase CRC bits to reduce noise. This requires modifications to existing receivers. 3) Two alternative codes. 4) Variable Pulse repetition rate (Long, short, repeat). All options can be implemented with ongoing ASIC design.	Simulations of post processing performance: A simple simulation of two double code tags with a code in common have been simulated with positive results without a need for significant changes in processing. Future simulations will add more realistic noise and a greater number of simultaneous tags. Tank simulation of receiver performance: Simulations are planned to evaluate receiver performance for coding options under tank conditions with simulated noise.	Concerns have been raised about the ability of third party equipment to be reconfigured to support increased code length and possibly additional barker codes.
Application space	None	None	None
ASIC/ Circuitry	Has received design kits for the Jazz Semiconductor 40V process and the On Semiconductor 80V process. Expects to receive the On Semiconductor 50V design kit shortly. Has chosen the ASIC operation range of 2-3 V and has created some test structures for the initial ASIC	Completed test structures for initial AISC Fabrication run on April 18.	None

Time period	Accomplishments 3/1/11 to 3/31/11	Planned Activities 4/1/11 to 4/30/11	Issues
Batteries	Continued measuring tag current and voltage characteristics to determine the battery requirements. Continued investigating the merits and drawbacks of cathode material for the new battery under development to meet or exceed the 337 battery: CFx , Silver vanadium oxide, Sulfides (MoS2, FeS2 etc.), Oxides (MnO2 etc.) Several coin cell batteries with the CFx cathode material with different binders were assembled to evaluate performance. The cell with the best performance was assembled with a tag and has been successfully running for 6+ days in ambient conditions. To aid in the ASIC first round test circuit build, an operating voltage of 2.0 – 3.0V was chosen.	Continue testing the new tags at different PRI and obtain the characteristics; Improve the material performance by making a hybrid composite with high capacity, energy and rate capability; Lithium primary battery assembly using Swagelok cells. Improve the material loading techniques – necessary for high loading in primary batteries.	None
Form/ packaging	Investigating the use of a Tefzel (Teflon) capsule for device packaging. Universal Plastics has been identified as a supplier of Tefzel capsules for initial testing. Pricing for custom dies to make this specific capsule and pricing per unit are reasonable; $2K for dies and with volume quantities < $1.00 per capsule.	Transmitter interference study: Will the capsule interfere with the tag signal. Larger capsules have been ordered to test for signal interference with current tags.	None
Ceramics/ Transducer	Performed resonance and frequency measurement on several PZT transducers.	Investigate the feasibility of the materials for JSATS tag frequency and source level	None

JSATS Tag downsize project progress report No. 3

Report Date: April 29, 2011

Prepared for: US Army Corps of Engineers, Portland District

Prepared by: Pacific Northwest National Laboratory

Comment: This is the third of a series of monthly progress reports on the conduct of the JSATS Tag downsize project. The purpose is to provide the Portland District with a periodic summary of accomplishments, planned activities, and issues.

Summary:

Time period	**Accomplishments** **4/1/11 to 4/30/11**	**Planned Activities** **5/1/11 to 5/31/11**	**Issues**
Code space	Ran basic tests of filtering algorithm on alternating codes and performance was acceptable. Current ASIC/Circuit design support all four proposed options.	Next step is tank testing to address the influence of noise.	
Application space	None	None	None
ASIC/ Circuitry	An initial test ASIC was submitted to Manufacturer on 4/19. The ASIC contained a number of test structures, including the voltage booster, oscillators, PZT driver, and temperature measurement circuit. We expect to receive fabricated parts back in June.	We will perform tests to evaluate the feasibility for programming the ASIC. We will also work on the design of the digital control logic that is necessary for a fully functional ASIC..	Although we will probably be ready to fabricate the first fully-functional ASIC in July, the next fabrication opportunity for our selected Fabrication vendor will most likely be in October or November. Although receipt of this ASIC will be delayed, the overall project schedule is not affected.
Batteries	Continued investigating the merits and drawbacks of cathode material for the new battery under development to	Continue assembly of the Swagelok cells and test their performance; Identify and solve the high impedance	None

Time period	Accomplishments 4/1/11 to 4/30/11	Planned Activities 5/1/11 to 5/31/11	Issues
	meet or exceed the 337 battery. Focused efforts on developing the Swagelok cell test vehicle assembly and characteristics. Swagelok batteries using CF_1 and CCF_1 cathode material have been assembled successfully. Initial test results are promising.	problem in the Swagelok cell; Improve the current collection efficiency of the Swagelok cell (use of conductive paste on the cathode is a possible solution); Evaluate Temperature performance of the coin cell over 0 – 30^{o}C range; Use CFx in a Swagelok cell and characterize it; Study the hybrid composite materials for improved performance.	
Form/ packaging	Investigating several packaging materials to provide the maximum transmitted energy. Talking with medical implant companies to ensure best packaging options for hermetic sealing.	Packaging materials for maximum transmitted energy study.	None
Ceramics/ Transducer	Ordered and received bare PZT transducers from several suppliers.	Evaluate the feasibility of the newly arrived materials and transducers for JSATS downsize tags.	None

JSATS Tag downsize project progress report No. 4

Report Date: May 31, 2011

Prepared for: US Army Corps of Engineers, Portland District

Prepared by: Pacific Northwest National Laboratory

Comment: This is the fourth of a series of monthly progress reports on the conduct of the JSATS Tag downsize project. The purpose is to provide the Portland District with a periodic summary of accomplishments, planned activities, and issues.

Summary:

Time period	**Accomplishments** **5/1/11 to 5/31/11**	**Planned Activities** **5/1/11 to 5/31/11**	**Issues**
Code space	Continue developing filtering algorithm on alternating codes and performance was acceptable.	Next step: run additional tank testing to address the influence of noise.	None
Application space	None	None	None
ASIC/ Circuitry	Preparation work is underway for testing the initial ASIC when it arrives back from vendor in mid-June. A test board is being designed and fabricated. We also have developed hardware description language (HDL) models of the ASIC control circuitry for both simulations and testing.	The primary activity next month will be testing the initial ASIC when it arrives. However, we will also continue working on the design and layout of the fully functional ASIC	None
Batteries	Investigated hybrid cathode materials that show high capacity for both high rate and low rate operation. Began experiments with a new battery test from that eliminates the high resistance problems encountered with the Swagelok test design. Conducted temperature	Continue assembly of pouch cells to test their characteristics; Lower the total weight of the pouch cell; Pouch cell assembly using high performance materials; Temperature variation in hybrid materials. New synthesis techniques for	None

Time period	Accomplishments 5/1/11 to 5/31/11	Planned Activities 5/1/11 to 5/31/11	Issues
	experiments that monitor battery voltage between 0 – 24 C.	CF_1 based materials. Other primary cathode materials.	
Form/ packaging	Located a Parylene vacuum deposition machine on site at PNNL. This next period will be devoted to permitting and installation into a class 1000 clean room. Initial calibration experiments for thickness and uniform 3D coating will be conducted on spare / old ASIC devices..	Parylene deposition machine permit and install; Order Parylene material; Calibration.	None
Ceramics/ Transducer	Started evaluating the feasibility of several newly arrived materials and transducers for JSATS downsize tags.	Order more candidate materials and continue evaluating received materials.	None

JSATS Tag downsize project progress report No. 5

Report Date: June 30, 2011

Prepared for: US Army Corps of Engineers, Portland District

Prepared by: Pacific Northwest National Laboratory

Comment: This is the fifth of a series of monthly progress reports on the conduct of the JSATS Tag downsize project. The purpose is to provide the Portland District with a periodic summary of accomplishments, planned activities, and issues.

Summary:

Time period	**Accomplishments** **6/1/11 to 6/30/11**	**Planned Activities** **6/1/11 to 6/30/11**	**Issues**
Code space	Developed an encoding algorithm on alternating codes with temperature measurement embedded within the tag codes.	Evaluate the encoding algorithm using simulated data and run additional tank testing.	None
Application space	None	None	None
ASIC/ Circuitry	Received the initial ASIC (version 0) submitted in April. Fabricated circuit boards for testing of the initial ASIC. Defined digital control specifications for next ASIC (version 1)	Test the initial ASIC. Will test most circuit components with unpackaged parts. Test driver circuit with PZT crystals after packaging.	None
Batteries	Improved the performance of self-made Pouch Cells and reduced its weight 139 mg from the initial 205 mg. Investigated the characteristics of the new Pouch Cells including peak current, capacity and service life.	Further reduce the weight by using better packaging materials. Continue testing the new batteries with current JSATS transmitters.	None
Form/ packaging	Completed installation and permitting of the Parylene vacuum deposition machine into a class 1000 clean room. Received Parylene material.	Calibration and training for Parylene Deposition. Continue searching for alternative packaging materials.	None

Time period	Accomplishments 6/1/11 to 6/30/11	Planned Activities 6/1/11 to 6/30/11	Issues
Ceramics/ Transducer	Evaluated several types of PZT with various sizes. It is possible to reduce PZT tube dimension by 15% while maintaining acceptable source level.	Order more candidate materials and continue evaluating received materials. Experiment with different backing materials. Study effect of PZT tube length on the tag source level.	None

JSATS Tag downsize project progress report No. 6

Report Date: July 31, 2011

Prepared for: US Army Corps of Engineers, Portland District

Prepared by: Pacific Northwest National Laboratory

Comment: This is the 6th of a series of monthly progress reports on the conduct of the JSATS Tag downsize project. The purpose is to provide the Portland District with a periodic summary of accomplishments, planned activities, and issues.

Summary:

Time period	**Accomplishments** **7/1/11 to 7/31/11**	**Planned Activities** **8/1/11 to 8/31/11**	**Issues**
Code space	Evaluated the encoding algorithm on alternating codes to make sure it is compatible with existing equipment.	Continue evaluating the encoding algorithm using simulated data and newly packaged ASIC.	None
Application space	None	None	None
ASIC/ Circuitry	Sent out Initial ASIC (Version 0) for package (2-wk turnaround). Developed strategy for auto-computing CRC. Decided on scheme for programming ASIC	Test the initial ASIC. Will test most circuit components with unpackaged parts. Test driver circuit with PZT crystals after packaging.	None
Batteries	Measured minimum output voltage of the new battery and its voltage variation over environment temperature. Evaluated high performance hybrid materials and their temperature characteristics using the current JSATS transmitters.	Continue evaluating other materials and other methods to make the battery lighter and tighter. Apply the other high performance cathode materials.	None
Form/ packaging	Evaluated the coating process of the current JSATS transmitters and got ready for initial depositions using in-house system.	Continue searching for alternative packaging materials. Perform initial depositions in house using old sensors and transducers.	None

Time period	Accomplishments 7/1/11 to 7/31/11	Planned Activities 8/1/11 to 8/31/11	Issues
Ceramics/ Transducer	Evaluated the source level of transducers using backing materials with various densities. Evaluated frequency response of PZT transducer.	Continue evaluating frequency response and effect of backing materials. Study effect of PZT tube length and orientation on source level.	None

JSATS Tag downsize project progress report No. 7

Report Date: August 31, 2011

Prepared for: US Army Corps of Engineers, Portland District

Prepared by: Pacific Northwest National Laboratory

Comment: This is the 7th of a series of monthly progress reports on the conduct of the JSATS Tag downsize project. The purpose is to provide the Portland District with a periodic summary of accomplishments, planned activities, and issues.

Summary:

Time period	**Accomplishments** **8/1/11 to 8/31/11**	**Planned Activities** **9/1/11 to 9/30/11**	**Issues**
Code space	Initiated discussions on future code space management for downsized transmitter.	Continue evaluating the encoding algorithm using simulated data and newly packaged ASIC.	None
Application space	None	None	None
ASIC/ Circuitry	Evaluated components of the initial ASIC (V0). Built test texture as a benchtop prototype of downsized transmitter for testing charge pump and driver circuit on ASIC and battery/PZT evaluations. Completed about 40% of Digital control circuitry design for ASIC V1.	Evaluate performance of driver circuit with actual PZT crystal. Compare performance of different PZT crystals. Optimize power consumption of driver circuit. Determine what driving voltage produces desired sound pressure level. Estimate total power consumption of final ASIC. Evaluate performance of new batteries against typical power profile.	None
Batteries	Evaluated power requirements of tags using different batteries. Ball milled different carbon additives with CF1 and studied their performance.	Test new light batteries (< 100 mg) for their performance. Optimize the conductive carbon content. Test other potential cathode materials.	None
Form/ packaging	Parylene Coater is now operational. Conducted	Continue parylene C deposition system testing and map	None

Time period	Accomplishments 8/1/11 to 8/31/11	Planned Activities 9/1/11 to 9/30/11	Issues
	test/calibration Runs using wire mount samples and low contact mount samples.	deposition yield. Fabricate 3D parts for test runs. Make silicon mold for intermediate layer. Order capsule parts once battery length finalized.	
Ceramics/ Transducer	Evaluated tag source level using different waveform shapes. Studied effect of PZT length on source level. Measured voltage response of different types of PZT.	Complete source level measurement for PZT of different lengths. Investigate how increase of drive voltage affects battery life. Build and test PZT-only prototype tags with parylene C coating.	None

JSATS Tag downsize project progress report No. 11

Report Date: January 11, 2012

Prepared for: US Army Corps of Engineers, Portland District

Prepared by: Pacific Northwest National Laboratory

Comment: This is the 11th of a series of monthly progress reports on the conduct of the JSATS Tag downsize project. The purpose is to provide the Portland District with a periodic summary of accomplishments, planned activities, and issues.

Summary:

Time period	**Accomplishments** **12/1/11 to 12/31/11**	**Planned Activities** **1/1/12 to 1/31/12**	**Issues**
Implantation assessment	Ready to start as soon as funding is available.	Finalize dummy tag design and manufacture dummy tags. Preliminary efforts to test needles, scalpel incisions and locations for insertion.	None
ASIC/ Circuitry	Fixed bugs with ASIC v0 test board; Fabricated new v0 test board that gives more accurate power consumption; Performed initial testing of RF programming circuit; Located manufacturing service to automate future circuit board assembly.	Fabricate 10-position circuit board for battery testing; Develop test board and miniature circuit board for ASIC v1; Continue discussions with circuit board manufacturer.	None
Batteries	Conducted performance testing of the new micro batteries combined with ASIC circuit. Achieved minimum tag life requirement.	Continue to improve the micro batteries manufacturing process. Continue to evaluate the ASIC board design using the lab-made micro batteries.	None
Form/ packaging	Tested the Tefzel battery capsule and found no significant weight loss or compatibility issues with all three components of battery	Continue Parylene C deposition system thickness mapping and epoxy injection design.	None

Time period	Accomplishments 12/1/11 to 12/31/11	Planned Activities 1/1/12 to 1/31/12	Issues
	capsule: Tefzel / epoxy / electrolyte.		
Ceramics/ Transducer	Obtained beam patterns for length-mode PZT with dual PZTs positioned at 30º angle with each other; Optimized the performance of the sound-wave reflector; Evaluated the performance of some smaller PZTs from two vendors.	Evaluate the performance (source level & energy consumption) of small PZTs with reflector; Evaluate the performance of PZT coated with Parylene-C and 3M epoxy; Evaluate new PZTs from additional vendors.	None
Code space	None	None.	None
Application space	None	None	